IN THE CLAIMS

1. (*Currently Amended*) A process for forming a contact for a semiconductor device comprising:

forming a first compound semiconductor layer, wherein: the first compound semiconductor material layer includes a first compound semiconductor material and has a first conductivity type;

forming a second compound semiconductor layer on the first semiconductor layer, wherein the second compound semiconductor layer includes a second compound semiconductor material and has a second conductivity type; and the second conductivity type is opposite the first conductivity type;

forming a third compound semiconductor layer on the second compound semiconductor layer, said third compound semiconductor layer of said first conductivity type, wherein the first, second and third layers are active layers in a transistor device;

patterning the third ~~second~~ semiconductor layer to define an opening therein with a wall, said opening exposing a portion of the second [first] active layer; and

forming a fourth ~~third~~ compound semiconductor material upon at least a portion of the exposed second [first] active layer and at least partially within the opening, wherein: the third compound semiconductor material ~~has an upper surface that is substantially co-planar with an upper surface of the second compound semiconductor layer,~~ has the second ~~first~~ conductivity type and a dopant concentration that is higher than a dopant concentration of the second ~~first~~ compound semiconductor layer; and ~~the third compound semiconductor material is electrically connected to the first compound semiconductor layer and is insulated from the second compound semiconductor layer.~~

2. (*Currently Amended*) The process of claim 1, wherein the fourth ~~third~~ compound semiconductor material is formed by sputtering.

3. (*Currently Amended*) The process of claim 1, wherein each of the first, second, third and fourth ~~and third~~ compound semiconductor materials include at least two Group IVA elements.

4. (*Currently Amended*) The process of claim 1, wherein each of the first, second, third and fourth ~~and third~~ compound semiconductor materials include silicon carbide.

5. (*Currently amended)* The process of claim 1, further comprising ~~forming a metal layer above and electrically connected to the third compound semiconductor material~~ forming a first metal contact of a first type of metal on the third semiconductor layer and forming a second metal contact of a second type of metal on the fourth semiconductor layer.

6. (*Currently Amended*) The process of claim 5, wherein an electrical connection between the third compound semiconductor material and the first metal layer is ohmic and an electrical connection between the fourth compound semiconductor and the second metal layer is ohmic.

7. (*Currently Amended*) The process of claim 5, wherein the first metal layer comprises aluminum and the second metal layer comprises nickel.

8. Cancelled

9. (*Currently Amended*) A semiconductor device comprising:

a first active layer including a first compound semiconductor material and having a first conductivity type;

a second active layer including a second compound semiconductor material and having a second conductivity type opposite the first conductivity type, wherein the second active layer contacts the first active layer;

a third active layer including a third compound semiconductor material and having the first conductivity type, wherein the third active layer contacts the second active layer, a combination of the first, second, and third active layer are at least part of a transistor;

an opening defined by said second and third active layers, said opening extending through the third active layer, said opening contacting and terminating within the second active layer;

a fourth compound semiconductor material at least partially within the opening and on the third active layer, wherein the fourth compound semiconductor material has the second conductivity type and a dopant concentration higher than the dopant concentration of the second active layer and is electrically connected to the second active layer~~, the fourth compound semiconductor material having an upper surface that is substantially coplanar with an upper surface of the third compound semiconductor layer~~; ~~and~~

an insulating layer at least partially within the opening, wherein the insulating layer lies between the third active layer and the fourth compound semiconductor material; and

a first metal contact of a first type of metal on the third semiconductor layer and forming a second metal contact of a second type of metal on the fourth semiconductor layer.

10. (*Original*) The device of claim 9, where each of the first, second, third, and fourth compound semiconductor material include at least two Group IVA elements.

11. (*Original*) The device of claim 9, where the first, second, third, and fourth compound semiconductor material comprise silicon carbide.

12. (*Original*) The device of claim 9, further comprising electrical contacts to the third active layer and the fourth compound semiconductor material.

13. (*Currently Amended*) The device of claim 12, wherein the metal layers are aluminum and nickel, respectively, and the electrical contacts are ohmic.

14. (*Currently amended*) The device of claim 13, wherein the device further comprises a second insulating layer on the surface of the third active layer ~~and surfaces of the second insulating layer and the metal contacts furthest from the substrate lie in substantially a same plane~~.

15. (*Original*) The device of claim 9, wherein the second active layer has a thickness in a range of approximately 0.1 - 2 microns thick.

16. (*Currently Amended*) A semiconductor device comprising:

a first active layer including a first compound semiconductor material and having a first conductivity type;

a second active layer including a second compound semiconductor material and having a second conductivity type opposite the first conductivity type, wherein the second active layer contacts the first active layer;

a third active layer including a third compound semiconductor material and having the first conductivity type, wherein the third active layer contacts the second active layer, a combination of the first, second, and third active layer are at least part of a transistor;

an opening defined by the second and third active layers, the opening extending through the third active layer, the opening terminating within and exposing a portion of the second active layer, sidewalls of the opening formed

by the third active layer, a bottom of the opening formed by the exposed portion of the second active layer;

an insulating layer at least partially within the opening and covering the sidewalls thereof; and

a fourth compound semiconductor material disposed within the opening upon the exposed portion of the second active layer upon the surface of the third compound semiconductor and upon the insulating layer covering the sidewalls thereof, the fourth compound semiconductor material having the second conductivity type and a dopant concentration higher than the dopant concentration of the second active layer and being electrically connected to the second active layer, the fourth compound semiconductor material substantially filling the opening and having an upper surface that is substantially coplanar with an upper surface of the third compound semiconductor layer.